REMARKS

Claims 1-12, 14-16 and 18-20 are pending in the present application. Claims 1-12, 14-16 and 18-20 have been rejected, and claims 1-4 are independent. Reconsideration in view of the following arguments is kindly requested.

Claim Rejections – 35 U.S.C. § 102

Claims 1-12, 14-16 and 18-20 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Surlekar, USP 5,668,764. This rejection is respectfully traversed.

Applicant submits that Surlekar fails to teach or disclose transferring internal signals externally from the integrated circuit device through data input/output pads, where the internal signals are used for addressing storage locations and controlling internal operations, as recited in claim 1.

Surlekar discloses a memory unit, which includes a data input/output buffer 16 coupled to a memory array 15, and which is configured to receive control signals from timing and control unit 19 and address signals from column address buffers 12. See Fig. 1 of Surlekar.

The Examiner alleges:

> "Surlekar teaches (Figure 1) data input/output buffer 16 that is transfers internal signals externally via data out register 17 as stated in the present application."

Applicant submits that nowhere does Surlekar teach or disclose transferring internal signals externally. The data input/output buffer 16 is configured to output data signals externally, which are input from memory array unit 15. See column 1, lines 35-42 of Surlekar. The data input/output buffer 16 receives internal data signals (i.e. control signals and address signals), and data from memory array 15 and register 18. However, nowhere does the specification of Surlekar recite transferring the internal signals externally. Instead, the signals from the column address buffers 12 and control unit 19 are used to control the operation of the data input/output buffer 16. Thus, Surlekar fails to teach or disclose transferring internal signals externally from the integrated circuit device through data input/output pads, where the internal signals are used for addressing storage locations and controlling internal operations, as recited in claim 1.

Accordingly, Applicant submits that claim 1 and those claims dependent thereon are allowable over the prior art. Withdrawal of this rejection is kindly requested.

Regarding claims 2-4, Applicants submit for similar reasons set forth above with regard to claim 1, that claims 2-4 and those claims dependent thereon are also allowable over the prior art. Withdrawal of the rejection to these claims is also kindly requested.

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of claims 1-12, 14-16 and 18-20 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By _____
John A. Castellano, Reg. No. 35,094

P.O. Box 8910
Reston, Virginia 20195
(703) 668-8000

JAC/KE:js